WHAT IS CLAIMED IS:

1. A semiconductor switching circuit device formed on a substrate, comprising:

a first, a second, a third and a fourth field-effect transistor, each of said transistors having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer of the substrate;

a first, a second, a third and a fourth input terminal pad corresponding to the first, second, third and fourth transistors, respectively, the source electrode or the drain electrode of each of the four transistors being connected to the corresponding input terminal pad thereof;

a first common output terminal pad connected to the source electrode or the drain electrode of the first transistor and connected to the source electrode or the drain electrode of the second transistor, the two electrodes of the first and second transistors which are connected to the first common output terminal pad not being connected to any of the input terminal pads;

a second common output terminal pad connected to the source electrode or the drain electrode of the third transistor and connected to the source electrode or the drain electrode of the fourth transistor, the two electrodes of the third and fourth transistors which are connected to the second common output terminal pad not being connected to any of the input terminal pads;

a first control terminal pad connected to the gate electrodes of the first and third transistors; and

a second control terminal pad connected to the gate electrodes of the second and fourth transistors.

2. The semiconductor switching circuit device of claim 1, wherein each of the gate electrodes forms a Schottky contact with the channel layer and each of the source electrodes and the drain electrodes forms an ohmic contact with the channel layer.

3. The semiconductor switching circuit device of claim 1, wherein the substrate is made of a compound semiconductor and each of the transistors is a metal-semiconductor field-effect transistor.

4. The semiconductor switching circuit device of claim 1, further comprising a first connection connecting the first control terminal pad and the gate electrode of the third transistor, wherein the four transistors are aligned in a direction forming a row of the first, second, third and fourth transistors in this order, and wherein the connection is disposed along the row of the transistors.

5. The semiconductor switching circuit device of claim 4, wherein the connection comprises a resistor formed between the first control terminal pad and the gate electrode of the third transistor.

6. The semiconductor switching circuit device of claim 4, wherein the substrate is made of a compound semiconductor and the resistor comprises a high dopant concentration region.

7. The semiconductor switching circuit device of claim 4, further comprising a second connection connecting the second control terminal pad and the gate electrode of the second transistor, wherein the two connections intersect each other.

8. The semiconductor switching circuit device of claim 4, wherein the first, second, third and fourth input terminal pads are disposed on one side of the device so that each of the pads is placed next to the corresponding transistor and wherein the first and second common output terminal pads and the first and second control terminal pads are disposed on a side of the device opposite the side of the device of the four input terminal pads so that the two control terminal pads are placed at both ends of said opposite side of the device and the two common output terminal pads are placed between the two control terminal pads.

9. The semiconductor switching circuit device of claim 7, wherein the first, second, third and fourth input terminal pads are disposed on one side of the device so that each of the pads is placed next to the corresponding transistor, wherein the first and second common output terminal pads and the first and second control terminal pads are disposed on a side of the device opposite the side of the device of the four input terminal pads so that the two control terminal pads are placed at both ends of said opposite side of the device and the two common output terminal pads are placed between the two control terminal pads, and wherein the first and second connections are disposed between the row of the four transistors and a row of the control terminal pads and the common output terminal pads.

10. The semiconductor switching circuit device of claim 8, wherein portions of the first and second transistors are disposed between the first and second input terminal pads, and wherein portions of the third and fourth transistors are disposed between the third and fourth input terminal pads.

11. The semiconductor switching circuit device of claim 4, wherein each of the gate electrodes forms a Schottky contact with the channel layer and each of the source electrodes and the drain electrodes forms an ohmic contact with the channel layer.

12. The semiconductor switching circuit device of claim 4, wherein the substrate is made of a compound semiconductor and each of the transistors is a metal-semiconductor field-effect transistor.

13. A switching device comprising:

a semiconductor chip formed on a substrate, said semiconductor chip comprising a first, a second, a third and a fourth input terminal pad, a first and a second common output terminal pad and a first and a second control terminal pad, said semiconductor chip having no more than two control terminal pads;

an insulating board having a conductor pattern thereon, said semiconductor chip being mounted on the conductor pattern;

a plurality of external electrodes, each of said external electrodes being connected to a corresponding terminal pad of the chip; and

a resin layer covering the chip and the insulating board;

wherein each of the external electrodes is disposed near the corresponding terminal pad so that the external electrodes are aligned substantially symmetrically with respect to a center line of the insulating board.

14. The switching device of claim 13, wherein

the semiconductor chip further comprises a first, a second, a third and a fourth field-effect transistor, each of said transistors having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer of the substrate,

the first, second, third and fourth input terminal pads are provided for the first, second, third and fourth transistors, respectively, the source electrode or the drain electrode of each of the four transistors being connected to the corresponding input terminal pad thereof,

the first common output terminal pad is connected to the source electrode or the drain electrode of the first transistor and is connected to the source electrode or the drain electrode of the second transistor, the two electrodes of the first and second transistors which are connected to the first common output terminal pad not being connected to any of the input terminal pads;

the second common output terminal pad is connected to the source electrode or the drain electrode of the third transistor and is connected to the source electrode or the drain electrode of the fourth transistor, the two electrodes of the third and fourth transistors which are connected to the second common output terminal pad not being connected to any of the input terminal pads;

the first control terminal pad is connected to the gate electrodes of the first and third transistors; and

the second control terminal pad is connected to the gate electrodes of the second and fourth transistors.

15. The switching device of claim 13, wherein the external electrodes are formed on a back side of the insulating board, said back side being opposite to the front side of the insulating board covered by the resin layer.

16. The switching device of claim 13, wherein the chip has only eight terminal pads, and wherein eight external electrodes are provided so that each of the eight terminal pads is connected to one of the eight external electrodes.

17. The switching device of claim 16, wherein the external electrodes for the four input terminal pads are aligned along one side of the insulating board with respect to said center line of symmetry, and wherein the external electrodes for the two control terminal pads and the two common output terminal pads are aligned along a side of the insulating board opposite the side of the external electrodes for the four input terminal pads with respect to said center line of symmetry.

18. The switching device of claim 14, wherein a marking is formed on a surface of the resin coating, said marking indicating a polarity of the external electrode.

19. A switching device comprising:

a semiconductor chip formed on a substrate, said semiconductor chip comprising a first, a second, a third and a fourth input terminal pad, a first and a second common output terminal pad and a first and a second control terminal pad, said semiconductor chip having no more than two control terminal pads;

an insulating resin film having a conductor pattern and the semiconductor chip embedded therein, said semiconductor chip being mounted on the conductor pattern; and

a plurality of external electrodes, each of said external electrodes being connected to

a corresponding terminal pad of the chip;

wherein each of the external electrodes is disposed near the corresponding terminal pad so that the external electrodes are aligned substantially symmetrically with respect to a center line of the insulating resin film.

20. The switching device of claim 19, wherein

the semiconductor chip further comprises a first, a second, a third and a fourth field-effect transistor, each of said transistors having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer of the substrate,

the first, second, third and fourth input terminal pads are provided for the first, second, third and fourth transistors, respectively, the source electrode or the drain electrode of each of the four transistors being connected to the corresponding input terminal pad thereof,

the first common output terminal pad is connected to the source electrode or the drain electrode of the first transistor and is connected to the source electrode or the drain electrode of the second transistor, the two electrodes of the first and second transistors which are connected to the first common output terminal pad not being connected to any of the input terminal pads;

the second common output terminal pad is connected to the source electrode or the drain electrode of the third transistor and is connected to the source electrode or the drain electrode of the fourth transistor, the two electrodes of the third and fourth transistors which are connected to the second common output terminal pad not being connected to any of the input terminal pads;

the first control terminal pad is connected to the gate electrodes of the first and third transistors; and

the second control terminal pad is connected to the gate electrodes of the second and fourth transistors.

21. The switching device of claim 19, wherein the external electrodes are formed

on a back side of the insulating resin film, the conductor pattern being contained in said back side of the insulating film.

22. The switching device of claim 19, wherein the chip has only eight terminal pads, and wherein eight external electrodes are provided so that each of the eight terminal pads is connected to one of the eight external electrodes.

23. The switching device of claim 22, wherein the external electrodes for the four input terminal pads are aligned along one side of the insulating resin film with respect to said center line of symmetry, and wherein the external electrodes for the two control terminal pads and the two common output terminal pads are aligned along a side of the insulating resin film opposite the side of the external electrodes of the four input terminal pads with respect to said center line of symmetry.

24. The switching device of claim 19, wherein a marking is formed on a surface of the insulating resin film, said marking indicating a polarity of the external electrode.

25. A semiconductor switching circuit device comprising:

a first switch comprising two field-effect transistors each having a source electrode, a gate electrode, a drain electrode and an input terminal pad, and a common output terminal pad for the two transistors of the first switch, the source electrode or the drain electrode of each of the two transistors of the first switch being connected to the common output terminal pad of the first switch, and the source electrode or the drain electrode of each of the two transistors of the first switch which are not connected to the common output terminal pad of the first switch being connected to the input terminal pad thereof;

a second switch comprising two field-effect transistors each having a source electrode, a gate electrode, a drain electrode and an input terminal pad, and a common output terminal pad for the two transistors of the second switch, the source electrode or the drain electrode of each of the two transistors of the second switch being connected to the

common output terminal pad of the second switch, and the source electrode or the drain electrode of each of the two transistors of the second switch which are not connected to the common output terminal pad of the second switch being connected to the input terminal pad thereof; and

two control terminal pads, one of the two control terminal pads being connected to a gate electrode of one of the two transistors of the first switch and a gate electrode of one of the two transistors of the second switch, and another of said two control terminal pads being connected to a gate electrode of another of the two transistors of the first switch and a gate electrode of another of the two transistors of the second switch.

26. The semiconductor switching circuit device of claim 25, wherein each of the first and second switch comprises a single pole double throw switch.

27. A semiconductor switching circuit device comprising:

four input terminal pads;

two common output terminal pads; and

no more than two control terminal pads.

28. The semiconductor switching circuit device of claim 27, wherein the four input terminal pads receive two pairs of balanced signals, and the two common output terminal pads output one of the two pairs of the balanced signals selected by signals applied to the two control terminal pads.